PATENT APPLICATION
DOCKET NO.: 200208009-1

LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the claims of the present patent application.

1. (Currently Amended) A system for compensating for skew in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where N/M ≥ 1, the system comprising:

a phase detector operable to detect a phase difference between said first clock signal and said second clock signal;

a skew state detector disposed in communication with said phase detector for generating a skew state signal which tracks a phase relationship between said first clock signal and said second clock signal relative to a zero point of a timing window corresponding to said second clock signal; and

a synchronizer control signal generator, responsive to said skew state signal, ~~operating to generate~~ for generating at least one control signal ~~to compensate for said skew between said second clock signal~~ according to a value of said skew state signal.

2. (Original) The system as recited in claim 1, wherein said skew state signal is operable to compensate for greater than one clock period difference between said first clock signal and said second clock signal.

3. (Currently Amended) The system as recited in claim 1, ~~wherein said skew state signal is operable to track said phase relationship between said first clock signal and said second clock signal based on the location of coincident edges of said first and second clock signals.~~ wherein said at least one control signal is used to facilitate data transfer between said first clock domain and said second clock domain.

4. (Currently Amended) The system as recited in claim [[3]] 1, wherein said ~~coincident edges comprise~~ zero point comprises an instance of coincident rising edges.

5. (Currently Amended) The system as recited in claim [[3]] 1, wherein said ~~coincident edges comprise~~ zero point comprises an instance of coincident falling edges.

6. (Original) The system as recited in claim 1, wherein said skew state detector generates said skew state signal (skew_state) in response to sampled clock signals (pd_b_cr and pd_b_cf) provided by said phase detector.

7. (Currently Amended) The system as recited in claim 1, wherein said at least one ~~synchronizer~~ control signal ~~is transmitted to synchronizer circuitry~~ comprises an indication whether a current data transfer contains valid data.

8. (Currently Amended) The system as recited in claim 1, wherein said at least one ~~synchronizer~~ control signal is selected from the signal group ~~consisting of~~ comprising c0_sel, c1_sel, core_sel, b2c_valid, c2b_valid, and c2b_valid_m.

9. (Currently Amended) A method for compensating for skew in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$, the method comprising:

determining ~~the position of coincident edges of~~ a phase difference between said first clock signal and said second clock signal relative to a zero point of a timing window corresponding to said second clock signal;

~~determining~~ deciding if a state transition is necessary based on ~~tracking the position of said coincident edges of said first and second clock signals~~ a result of said determining step; and

generating a control signal indicative of said state transition, thereby compensating for said skew between said first clock signal and said second clock signal.

10. (Currently Amended) The method as recited in claim 9, wherein the operation of determining ~~the position of coincident edges comprises determining~~ a phase difference between said first clock signal and said second clock signal determines the phase difference to be at least one quarter cycle apart.

11. (Original) The method as recited in claim 9, wherein said state transition comprises a transition that tracks a negative skew difference between said first and second clock signals.

12. (Original) The method as recited in claim 9, wherein said state transition comprises a transition that tracks a positive skew difference between said first and second clock signals.

13. (Original) The method as recited in claim 9, wherein said control signal is operable to indicate that no skew state transition is necessary.

14. (Original) The method as recited in claim 9, wherein said control signal is indicative of a temporal relationship between said coincident edges and said second clock signal.

15. (Currently Amended) A computer system having an apparatus for compensating for skew in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where N/M ≥ 1, the computer system comprising:

means for determining ~~the position of coincident edges of~~ a phase difference between said first clock signal and said second clock signal relative to a zero point of a timing window corresponding to said second clock signal;

means for ~~determining~~ deciding if a state transition is necessary based on ~~tracking the position of said coincident edges of said first and second clock signals~~ a result of said determining; and

means for generating a control signal indicative of said state transition, thereby compensating for said skew between said first clock signal and said second clock signal.

16. (Currently Amended) The computer system as recited in claim 15, wherein said means for determining ~~the position of coincident edges further comprises~~ a phase difference between said first clock signal and said second clock signal comprises means for determining said first clock signal and said second clock signal to be at least one quarter cycle apart.

17. (Original) The computer system as recited in claim 15, wherein said state transition comprises a transition that tracks a negative skew difference between said first and second clock signals.

18. (Original) The computer system as recited in claim 15, wherein said state transition comprises a transition that tracks a positive skew difference between said first and second clock signals.

19. (Original) The computer system as recited in claim 15, wherein said control signal is operable to indicate that no skew state transition is necessary.

20. (Original) The computer system as recited in claim 15, wherein said control signal is indicative of a temporal relationship between said coincident edges and said second clock signal.